In the Specification:

Please replace the paragraph beginning on page 6, line 11 with the following amended paragraph:

According to still another aspect of the present invention, there is provided a thin film transistor substrate comprising: a substrate; a first transistor structure having a first semiconductor layer formed on the substrate, a first gate insulating film and a first gate electrode, wherein a channel region of the first semiconductor layer under the first gate electrode is intentionally doped with only p-type impurities, the first semiconductor layer includes n-type LDD regions outside the channel region and high impurity concentration n-type source/drain regions outside the n-type LDD regions, and the first gate electrode is made of a second metal layer; a second transistor structure having a second semiconductor layer formed on the substrate, a second gate insulating film and a second gate electrode, wherein a channel region of the second semiconductor layer under the second gate electrode is intentionally doped with p-type impurities at the first impurity concentration, the second semiconductor layer includes high impurity concentration n-type source/drain regions outside the channel region, and the second gate electrode is made of the second metal layer; and a third transistor structure having a third semiconductor layer formed on the substrate, a third gate insulating film and a third gate electrode, wherein a channel region of the third semiconductor layer under the third gate electrode is intentionally doped with p-type impurities at a second impurity concentration lower than the first impurity concentration, the

third semiconductor layer includes high impurity concentration p-type source/drain regions outside the channel region, and the third gate electrode is made of a ~~first~~ second metal layer ~~having etching characteristics~~ that is different from ~~etching characteristics of~~ the first metal layer.